HOLTEK

## 24-Bit A/D Peripheral

# BH45B1225

Revision: V1.40 Date: August 08, 2025

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# Table of Contents

## Features

- Wide operating voltage: 2.4V~5.5V
- Internal Programmable Gain Amplifier
- Internal $I^2C$ interface for external communiation
- 5Hz~1.6kHz ADC output data rate
- Internal temperature sensor for compensation
- Package Types: 8-pin SOP/16-pin NSOP

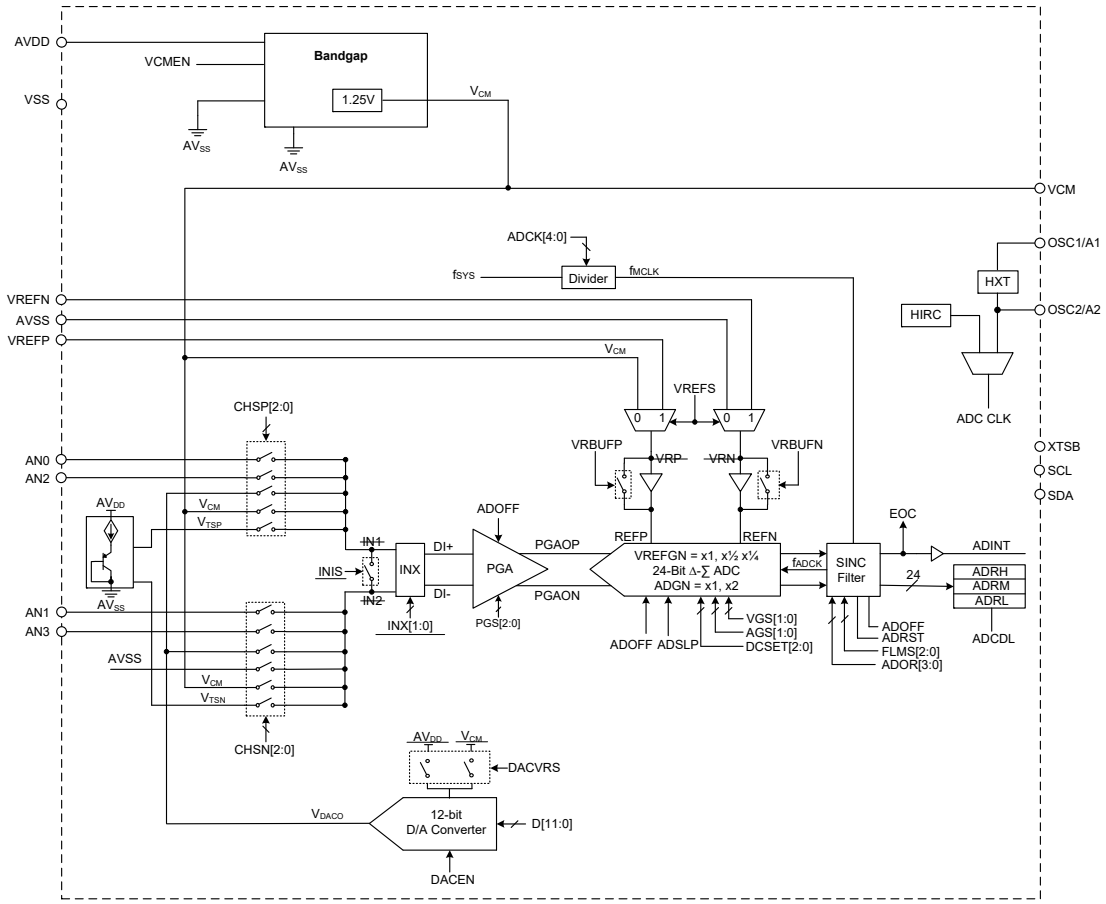
## Applications

- Instrumentation
- Health Monitoring Equipment
- Precision Sensing

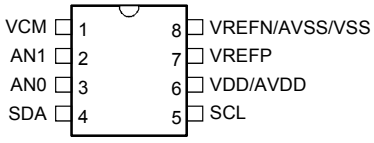
## General Description

The BH45B1225 is a multi-channel 24-bit Delta Sigma A/D converter which includes a programmable gain amplifier and is designed for applications that interface differentially to analog signals. The device has the benefits of low noise and high accuracy and communicates with external hardware using an internal $I^2C$ bus. This highly functionally integrated Delta Sigma analog to digital converter with its high accuracy and low power specifications offers a superior solution for interfacing to external sensors especially for battery powered applications.

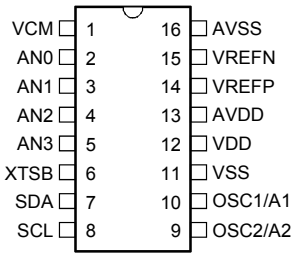
## Block Diagram




## Pin Assignment




**BH45B1225**
**8 SOP-A**




**BH45B1225**
**16 NSOP-A**

## Pin Description

| Pin Name | Type | Description |
|---|---|---|
| AN0 | AI | ADC input channel 0 |
| AN1 | AI | ADC input channel 1 |
| AN2 | AI | ADC input channel 2 |
| AN3 | AI | ADC input channel 3 |
| VERFP | AI | Positive reference input voltage |
| VERFN | AI | Negative reference input voltage |
| SCL | I | I²C clock line |
| SDA | I/O | I²C data line |
| XTSB | I | Low: external crystal, High: internal oscillator |
| OSC1/A1 | OSC | Oscillator input |
| | I | I²C slave address select |
| OSC2/A2 | OSC | Oscillator output |
| | I | I²C slave address select |
| VCM | AO | ADC internal common mode voltage output |
| VDD | PWR | Digital power supply |
| AVDD | PWR | Analog power supply |
| VSS | PWR | Digital negative power supply |
| AVSS | PWR | Analog negative power supply |

Legend: I: Digital Input; I/O: Digital Input/Output;
AI: Analog Input; AO: Analog Output;
OSC: Oscillator; PWR: Power.

## Absolute Maximum Ratings

Supply Voltage ..... $V_{SS}$-0.3V to$V_{SS}$+6.0V
Input Voltage ..... $V_{SS}$-0.3V to $V_{DD}$+0.3V
Storage Temperature..... -60°C to 150°C
Operating Temperature..... -40°C to 85°C
$I_{OL}$ Total ..... 80mA
$I_{OH}$ Total..... -80mA
Total Power Dissipation ..... 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## D.C. Characteristics

Operating Temperature: -40°C to 85°C, Ta=25°C, Typical

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{DD}$ | Operating Voltage (HXT) | — | $f_{SYS}=f_{HXT}$=4MHz | 2.4 | — | 5.5 | V |
| | | | $f_{SYS}=f_{HXT}$=8MHz | 2.4 | — | 5.5 | V |
| | | | $f_{SYS}=f_{HXT}$=12MHz | 2.4 | — | 5.5 | V |
| | Operating Voltage (HIRC) | — | $f_{SYS}=f_{HIRC}$=4.9152MHz | 2.4 | — | 5.5 | V |
| $I_{DD}$ | Operating Current (HXT) | 3V | No load, all peripherals off, $f_{SYS}=f_{HXT}$=4MHz | — | 500 | 750 | μA |
| | | 5V | | — | 1 | 1.5 | mA |
| | Operating Current (HIRC) | 3V | No load, all peripherals off, $f_{SYS}=f_{HIRC}$=4.9152MHz | — | 400 | 600 | μA |
| | | 5V | | — | 0.8 | 1.2 | mA |
| $I_{STB}$ | Standby Current | 3V | No load, all peripherals off | — | — | 1 | μA |
| | | 5V | | — | — | 2 | μA |
| $R_{PH}$ | Pull-high resistance for Input Ports (XTSB, A1, A2) | 3V | — | 20 | 60 | 100 | kΩ |
| | | 5V | — | 10 | 30 | 50 | kΩ |

## A.C. Characteristics

Operating Temperature: -40°C to 85°C, Ta=25°C, Typical

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $f_{SYS}$ | System Clock (HXT) | 2.4V~5.5V | $f_{SYS}=f_{HXT}$=4MHz | — | 4 | — | MHz |
| | | 2.4V~5.5V | $f_{SYS}=f_{HXT}$=8MHz | — | 8 | — | MHz |
| | System Clock (HIRC) | 2.4V~5.5V | $f_{SYS}=f_{HIRC}$=4.9152MHz | — | 4.9152 | — | MHz |
| $f_{HIRC}$ | High Speed Internal RC Oscillator (HIRC) | 3V | Ta=25°C | -2% | 4.9152 | +2% | MHz |
| | | 3V±0.3V | Ta=0°C~70°C | -5% | 4.9152 | +5% | MHz |
| | | 3V±0.3V | Ta=-40°C~85°C | -10% | 4.9152 | +10% | MHz |
| | | 2.4V~5.5V | Ta=0°C~70°C | -7% | 4.9152 | +7% | MHz |
| | | 2.4V~5.5V | Ta=-40°C~85°C | -10% | 4.9152 | +10% | MHz |

## I²C Electrical Characteristics

Operating Temperature: -40°C to 85°C, Ta=25°C, Typical

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $f_{I2C}$ | I²C Standard Mode (100kHz) $f_{SYS}$ Frequency | — | No clock debounce | 2 | — | — | MHz |
| | | — | 2 system clock debounce | 4 | — | — | MHz |
| | | — | 4 system clock debounce | 8 | — | — | MHz |
| | I²C Fast Mode (400kHz) $f_{SYS}$ Frequency | — | No clock debounce | 5 | — | — | MHz |
| | | — | 2 system clock debounce | 10 | — | — | MHz |
| | | — | 4 system clock debounce | 20 | — | — | MHz |

## D/A Converter Electrical Characteristics

Operating Temperature: -40°C to 85°C, Ta=25°C, Typical

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{DACO}$ | Output Voltage Range | — | — | $V_{SS}$ | — | $V_{REF}$ | V |
| $V_{REF}$ | Reference Voltage | — | — | 1.25 | — | $V_{DD}$ | V |
| $I_{DAC}$ | Additional Current for DAC Enable | — | $V_{REF}$=5V | — | — | 450 | μA |
| DNL | Differential Non-linearity | — | 2.4V ≤ $V_{DD}$ ≤ 5.5V | — | — | ±6 | LSB |
| INL | Integral Non-linearity | — | 2.4V ≤ $V_{DD}$ ≤ 5.5V | — | — | ±12 | LSB |

## PGA+ADC+VCM Electrical Characteristics

$V_{DD}$=$AV_{DD}$, Operating temperature: -40°C to 85°C, Ta=25°C, Typical

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $AV_{DD}$ | Supply Voltage for VCM, ADC, PGA | — | — | 2.4 | — | 5.5 | V |
| $V_{OUT\_VCM}$ | VCM Output Voltage (VCM Pin) | — | $AV_{DD}$=3.3V, No load | - 5% | 1.25 | +5% | V |
| $TC_{VCM}$ | VCM Temperature Coefficient | — | Ta=-40°C~85°C, $AV_{DD}$=3.3V, $I_{LOAD}$=10μA | — | — | 0.24 | mV/°C |
| $\Delta V_{LINE\_VCM}$ | VCM Line Regulation | — | 2.4V ≤ $AV_{DD}$ ≤ 3.3V, No load | — | — | 0.4 | %/V |
| $t_{VCMS}$ | VCM Turn-on Stable Time | — | $AV_{DD}$=3.3V, No load | — | — | 10 | ms |
| $I_{OH}$ | Source Current for VCM Pin | — | $AV_{DD}$=3.3V, $\Delta V_{OUT\_VCM}$= -2% | 3 | — | — | mA |
| $I_{OL}$ | Sink Current for VCM Pin | — | $AV_{DD}$=3.3V, $\Delta V_{OUT\_VCM}$= +2% | 3 | — | — | mA |
| **ADC & ADC Internal Reference Voltage (Sigma Delta ADC)** | | | | | | | |
| $I_{ADC}$ | Additional Current for ADC Enable | — | VCM enable, VRBUFP=1 and VRBUFN=1 | — | — | 1120 | μA |
| | | | VCM enable, VRBUFP=0 and VRBUFN=0 | — | 820 | 970 | μA |
| | | | VCM disable, VRBUFP=0 and VRBUFN=0 | — | 500 | 650 | μA |
| $I_{ADSTB}$ | Standby Current | — | System HALT, no load | — | — | 1 | μA |
| $RS_{ADC}$ | Resolution | — | — | — | — | 24 | bit |
| INL | Integral Non-linearity | — | $AV_{DD}$=3.3V, $V_{REF}$=1.25V, ΔSI=±450mV, PGA Gain=1 | — | ±50 | — | ppm |
| NFB | Noise Free Bits | — | $V_{REF}$=2.5V, Gain=32, Data rate=10Hz | — | 18.0 | — | Bit |
| | | | $V_{REF}$=2.5V, Gain=64, Data rate=10Hz | — | 17.4 | — | Bit |
| | | | $V_{REF}$=2.5V, Gain=128, Data rate=10Hz | — | 16.7 | — | Bit |
| ENOB | Effective Number of Bits | — | $V_{REF}$=2.5V, Gain=32, Data rate=10Hz | — | 20.7 | — | Bit |
| | | | $V_{REF}$=2.5V, Gain=64, Data rate=10Hz | — | 20.1 | — | Bit |
| | | | $V_{REF}$=2.5V, Gain=128, Data rate=10Hz | — | 19.4 | — | Bit |
| $f_{ADCK}$ | ADC Clock Frequency | — | — | 40 | 409.6 | 440 | kHz |
| $f_{ADO}$ | ADC Output Data Rate | — | $f_{MCLK}$=4.9152MHz, FLMS[2:0]=000B | 5 | — | 640 | Hz |
| | | | $f_{MCLK}$=4.9152MHz, FLMS[2:0]=010B | 12.5 | — | 1600 | Hz |

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{REFP}$ | External Reference Input Voltage | — | VREFS=1, VRBUFP=0, VRBUFN=0 | $V_{REFN}$+1 | — | $AV_{DD}$ | V |
| $V_{REFN}$ | | — | | 0 | — | $V_{REFP}$-1 | V |
| $V_{REF}$ | | — | $V_{REF}=(V_{REFP}–V_{REFN})×VGS$ | 1 | — | $AV_{DD}/2$ | V |
| **PGA** | | | | | | | |
| $V_{CM\_PGA}$ | Common Mode Voltage Range | — | — | 0.4 | — | $AV_{DD}$ -0.95 | V |
| $\Delta D_I$ | Differentail Input Voltage Range | — | Gain=PGS×AGS, $\Delta D_i$=DI+ - DI- | -$V_{REF}$/ Gain | — | +$V_{REF}$/ Gain | V |
| **Temperature Sensor** | | | | | | | |
| TCTS | Temperature Sensor Temperature Coefficient | — | Ta=-40°C~85°C, $V_{REF}$=1.25V, VGS[1:0]=00B (Gain=1), VRBUFP=0, VRBUFN=0 | — | 175 | — | μV/°C |

### Effective Number of Bits (ENOB)

$V_{REF}$=2.5V, $f_{ADCK}$=163kHz

| Data Rate (SPS) | PGA Gain | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 5 | 21.5 | 21.2 | 21.1 | 21.1 | 21.0 | 20.9 | 20.4 | 19.6 |
| 10 | 21.2 | 21.0 | 21.0 | 20.9 | 20.8 | 20.7 | 20.1 | 19.4 |
| 20 | 21.1 | 20.7 | 20.7 | 20.6 | 20.5 | 20.3 | 19.7 | 18.9 |
| 40 | 20.6 | 20.5 | 20.4 | 20.2 | 20.1 | 19.9 | 19.2 | 18.5 |
| 80 | 20.2 | 20.1 | 20.0 | 19.9 | 19.8 | 19.5 | 18.8 | 18.0 |
| 160 | 19.7 | 19.5 | 19.5 | 19.4 | 19.3 | 19.0 | 18.4 | 17.6 |
| 320 | 19.1 | 18.9 | 18.9 | 18.8 | 18.7 | 18.5 | 17.9 | 17.1 |
| 640 | 18.6 | 18.4 | 18.4 | 18.3 | 18.3 | 18.0 | 17.4 | 16.6 |

$V_{REF}$=2.5V, $f_{ADCK}$=409kHz

| Data Rate (SPS) | PGA Gain | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 12.5 | 21.9 | 21.4 | 21.4 | 21.3 | 21.1 | 20.7 | 19.9 | 19.2 |
| 25 | 21.6 | 21.1 | 21.1 | 21.0 | 20.9 | 20.4 | 19.6 | 18.8 |
| 50 | 21.2 | 20.9 | 20.8 | 20.7 | 20.4 | 19.9 | 19.2 | 18.3 |
| 100 | 20.8 | 20.5 | 20.4 | 20.3 | 20.0 | 19.5 | 18.8 | 17.9 |
| 200 | 20.3 | 19.7 | 19.7 | 19.6 | 19.4 | 18.9 | 18.2 | 17.4 |
| 400 | 19.3 | 19.0 | 19.0 | 18.9 | 18.8 | 18.4 | 17.8 | 16.9 |
| 800 | 18.8 | 18.6 | 18.6 | 18.5 | 18.3 | 17.9 | 17.2 | 16.5 |
| 1600 | 18.4 | 18.2 | 18.2 | 18.1 | 17.9 | 17.4 | 16.8 | 16.1 |

$V_{REF}$=1.65V, $f_{ADCK}$=163kHz

| Data Rate (SPS) | PGA Gain | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 5 | 21.5 | 21.2 | 21.2 | 21.1 | 20.9 | 20.5 | 20.0 | 19.2 |
| 10 | 21.3 | 21.0 | 20.9 | 20.7 | 20.5 | 20.2 | 19.5 | 18.7 |
| 20 | 20.9 | 20.6 | 20.5 | 20.4 | 20.2 | 19.8 | 19.1 | 18.3 |
| 40 | 20.4 | 20.1 | 20.1 | 20.0 | 19.8 | 19.4 | 18.8 | 18.0 |
| 80 | 19.8 | 19.5 | 19.5 | 19.4 | 19.2 | 18.8 | 18.2 | 17.5 |
| 160 | 19.3 | 19.0 | 19.0 | 18.9 | 18.7 | 18.4 | 17.8 | 17.0 |
| 320 | 18.8 | 18.5 | 18.5 | 18.4 | 18.3 | 17.9 | 17.3 | 16.5 |
| 640 | 18.3 | 18.1 | 18.1 | 18.0 | 17.8 | 17.5 | 16.8 | 16.0 |

$V_{REF}$=1.65V, $f_{ADCK}$=409kHz

| Data Rate (SPS) | PGA Gain | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 12.5 | 21.8 | 21.4 | 21.2 | 21.1 | 20.7 | 20.3 | 19.5 | 18.6 |
| 25 | 21.4 | 21.1 | 20.9 | 20.7 | 20.3 | 19.7 | 19.0 | 18.2 |
| 50 | 20.9 | 20.6 | 20.5 | 20.3 | 19.9 | 19.4 | 18.6 | 17.7 |
| 100 | 20.4 | 20.2 | 20.0 | 19.8 | 19.4 | 18.9 | 18.1 | 17.3 |
| 200 | 19.8 | 19.4 | 19.3 | 19.2 | 18.9 | 18.4 | 17.7 | 16.8 |
| 400 | 19.0 | 18.8 | 18.7 | 18.6 | 18.4 | 17.8 | 17.2 | 16.3 |
| 800 | 18.7 | 18.4 | 18.3 | 18.2 | 17.9 | 17.4 | 16.7 | 15.8 |
| 1600 | 18.2 | 18.0 | 17.9 | 17.7 | 17.3 | 16.7 | 16.2 | 15.4 |

$V_{REF}$=1.2V, $f_{ADCK}$=163kHz

| Data Rate (SPS) | PGA Gain | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 5 | 20.6 | 20.4 | 20.4 | 20.3 | 20.3 | 20.1 | 19.6 | 18.9 |
| 10 | 20.5 | 20.3 | 20.3 | 20.2 | 20.0 | 19.9 | 19.2 | 18.4 |
| 20 | 20.3 | 19.9 | 19.9 | 19.8 | 19.7 | 19.4 | 18.8 | 18.0 |
| 40 | 19.8 | 19.5 | 19.5 | 19.4 | 19.2 | 18.9 | 18.3 | 17.5 |
| 80 | 19.3 | 19.1 | 19.1 | 19.0 | 18.8 | 18.5 | 17.8 | 17.0 |
| 160 | 19.0 | 18.8 | 18.7 | 18.6 | 18.3 | 18.0 | 17.4 | 16.5 |
| 320 | 18.5 | 18.2 | 18.2 | 18.1 | 17.8 | 17.5 | 16.9 | 16.1 |
| 640 | 17.9 | 17.7 | 17.7 | 17.6 | 17.3 | 17.0 | 16.4 | 15.6 |

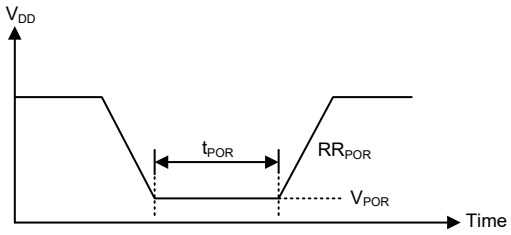
$V_{REF}$=1.2V, $f_{ADCK}$=409kHz

| Data Rate (SPS) | PGA Gain | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 12.5 | 20.9 | 20.7 | 20.5 | 20.3 | 20.1 | 19.8 | 19.1 | 18.2 |
| 25 | 20.7 | 20.4 | 20.2 | 20.1 | 19.8 | 19.4 | 18.6 | 17.8 |
| 50 | 20.3 | 20.1 | 19.8 | 19.7 | 19.4 | 18.8 | 18.1 | 17.4 |
| 100 | 19.9 | 19.6 | 19.4 | 19.2 | 18.9 | 18.4 | 17.7 | 16.8 |
| 200 | 19.5 | 19.2 | 19.0 | 18.8 | 18.5 | 17.9 | 17.2 | 16.4 |
| 400 | 18.9 | 18.7 | 18.6 | 18.4 | 18.0 | 17.5 | 16.7 | 15.9 |
| 800 | 18.5 | 18.2 | 18.0 | 17.8 | 17.5 | 16.9 | 16.2 | 15.4 |
| 1600 | 17.9 | 17.6 | 17.5 | 17.3 | 16.9 | 16.4 | 15.7 | 14.9 |

## Power-on Reset Electrical Characteristics

Operating Temperature: -40°C to 85°C, Ta=25°C, Typical

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{POR}$ | $V_{DD}$ Start Voltage to Ensure Power-on Reset | — | — | — | — | 100 | mV |
| $RR_{POR}$ | $V_{DD}$ Rising Rate to Ensure Power-on Reset | — | — | 0.035 | — | — | V/ms |
| $t_{POR}$ | Minimum Time for $V_{DD}$ Stays at $V_{POR}$ to Ensure Power-on Reset | — | — | 1 | — | — | ms |




## Functional Description

The BH45B1225 is a high accuracy multi-channel 24-bit Delta Sigma type analog-to-digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into a 24-bit digital value. In addition to the core analog to digital converter circuitry, the device also includes an internal Programmable Gain Amplifier PGA. The PGA gain control, ADC gain control and ADC reference gain control determine the overall amplification gain for ADC input signal, giving users a flexible way of setting up an overall gain to achieve an optimum amplification of the input signal for their specific applications. The converter has a total of four inputs allowing the formation of two differential input channels. The converter output is filtered via a SINC filter and the result stored as a 24-bit value in three data registers. An internal voltage regulator and reference sources are also included as well as a temperature sensor for A/D converter compensation due to temperature effects.

### Internal Registers

The device is setup and operated using a series of internal registers. Device commands and data are written to and read from the device using its internal $I^2C$ bus. This list provides a summary of all internal registers, their detailed operation is described under their relevant section in the functional description.

#### Register Initial Values

The following table shows the internal value of the individual register after a power on reset.

| Register | Power On Reset Value |
|---|---|
| PWRC | 0000 0000 |
| PGAC0 | -000 0000 |
| PGAC1 | -000 000- |
| PGACS | --00 0000 |
| ADRL | xxxx xxxx |
| ADRM | xxxx xxxx |
| ADRH | xxxx xxxx |
| ADCR0 | 0010 0000 |
| ADCR1 | 0000 000- |

| Register | Power On Reset Value |
|---|---|
| ADCS | - - - 0 0 0 0 0 |
| ADCTE | 1 1 1 0 0 1 0 0 |
| DAH | 0 0 0 0 0 0 0 0 |
| DAL | - - - - 0 0 0 0 |
| DACC | 0 0 - - - - - - |
| SIMC0 | 0 - - - 0 0 - - |
| SIMTOC | 0 0 0 0 0 0 0 0 |
| HIRCC | - - - - - 0 0 1 |
| HXTC | - - - - - 0 0 0 |

Note: "-" stands for Not implemented
"x" stands for Unknown

| Address | Register Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00H | PWRC | VCMEN | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01H | PGAC0 | — | VGS1 | VGS0 | AGS1 | AGS0 | PGS2 | PGS1 | PGS0 |
| 02H | PGAC1 | — | INIS | INX1 | INX0 | DCSET2 | DCSET1 | DCSET0 | — |
| 03H | PGACS | — | — | CHSN2 | CHSN1 | CHSN0 | CHSP2 | CHSP1 | CHSP0 |
| 04H | ADRL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05H | ADRM | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 06H | ADRH | D23 | D22 | D21 | D20 | D20 | D19 | D18 | D17 |
| 07H | ADCR0 | ADRST | ADSLP | ADOFF | ADOR3 | ADOR2 | ADOR1 | ADOR0 | VREFS |
| 08H | ADCR1 | FLMS2 | FLMS1 | FLMS0 | VRBUFN | VRBUFP | ADCDL | EOC | — |
| 09H | ADCS | — | — | — | ADCK4 | ADCK3 | ADCK2 | ADCK1 | ADCK0 |
| 0AH | ADCTE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0BH | DAH | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 |
| 0CH | DAL | — | — | — | — | D3 | D2 | D1 | D0 |
| 0DH | DACC | DACEN | DACVRS | — | — | — | — | — | — |
| 0EH | SIMC0 | SIMS | — | — | — | SIMDEB1 | SIMDEB0 | — | — |
| 10H | SIMTOC | SIMTOEN | SIMTOF | SIMTOS5 | SIMTOS4 | SIMTOS3 | SIMTOS2 | SIMTOS1 | SIMTOS0 |
| 11H | HIRCC | — | — | — | — | — | HIRCO | HIRCF | HIRCEN |
| 12H | HXTC | — | — | — | — | — | HXTM | HXTF | HXTEN |

## Internal Power Supply

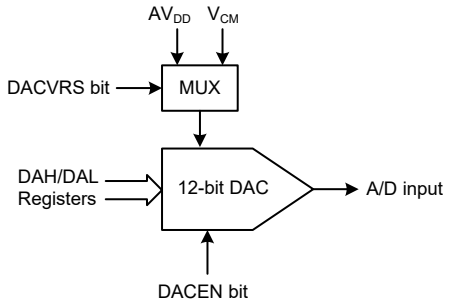
This device contains the VCM for the regulated power supply. The $V_{CM}$ can be used as the reference voltage for ADC module. The VCM function is controlled by the VCMEN bit and can be powered off to reduce the power consumption.

## Reference Voltages

An internal voltage reference source, known as the $V_{CM}$, is used as a converter reference. The $V_{CM}$ is sourced from a bandgap reference generator thus providing a temperature stable reference and has a output voltage level fixed at 1.25V. The VCM function is controlled by the VCMEN bit and can be switched off to reduce the power consumption.

The converter reference voltage range is supplied on two external reference pins, VREFP and VREFN. These offer a full reference voltage range of $AV_{SS}$ to $AV_{DD}$. This externally supplied reference voltage can be attenuated by 0.5 or 0.25 using the VGS1~VGS0 bits in the PGAC0 register.

An internal DAC is also provided as an additional reference voltage source. The DAC has two reference voltages which define the maximum value, supplied by either $AV_{DD}$ or $V_{CM}$. The DAC 12-bit value is setup using two data registers, DAL and DAH and the reference voltage is selected using the DACVRS bit in the DACC register. The overall enable bit for the DAC is the DACEN bit in the DACC register.




**• DAH Register − 0BH**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~0 **D11~D4**: DAC output control code

**• DAL Register − 0CH**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | D3 | D2 | D1 | D0 |
| R/W | — | — | — | — | R/W | R/W | R/W | R/W |
| POR | — | — | — | — | 0 | 0 | 0 | 0 |

Bit 7~4 Unimplemented, read as "0"

Bit 3~0 **D3~D0**: DAC output control code

Note: writing to this register only writes to a shadow buffer. Not until data is written to the DAH register will the actual data be written into the DAL register.

**• DACC Register − 0DH**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DACEN | DACVRS | — | — | — | — | — | — |
| R/W | R/W | R/W | — | — | — | — | — | — |
| POR | 0 | 0 | — | — | — | — | — | — |

Bit 7 **DACEN**: DAC enable or disable control bit
0: Disable
1: Enable

Bit 6 **DACVRS**: DAC reference voltage selection
0: DAC reference voltage sourced from $AV_{DD}$
1: DAC reference voltage sourced from $V_{CM}$

Bit 5~0 Unimplemented, read as "0"

## Power and Reference Control

The following table shows the overall control of the power and voltage sources.

| Control Bit | | Output Voltage | |
|---|---|---|---|
| ADOFF | VCMEN | Bandgap | VCM |
| 1 | 0 | Off | Disable |
| 1 | 1 | On | Enable |
| 0 | 0 | On | Disable |
| 0 | 1 | On | Enable |

**Power Control Table**

### Power Control Registers

- **PWRC Register − 00H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | VCMEN | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **VCMEN**: VCM function enable control
0: Disable
1: Enable
If the VCM is disabled, there will be no power consumption and VCM output pin is floating.

Bit 6~0 **D6~D0**: Performance optimizing bits
010_1000B: when ADCR1[FLMS2~0]=000B ($f_{ADCK}=f_{MCLK}/30$)
011_1100B: when ADCR1[FLMS2~0]=010B ($f_{ADCK}=f_{MCLK}/12$)
Others: reserved

## Oscillators

There are two kinds of oscillators used in this device, a fully internal oscillator and an external crystal oscillator. The device can operate using both the internal oscillator or an external crystal oscillator, selecting which oscillator is used is determined by the XTSB pin.

| XTSB Pin | Oscillator Type |
|---|---|
| 0 | External Crystal |
| 1 | Internal Oscillator |

### Oscillator Control Registers

There are two control registers for the device oscillators, one for the internal oscillator and one for the external oscillator. Which oscillator is used in the device is determined by the XTSB pin. Note that if the HIRC oscillator is selected then a full 16 clock cycle time is required for the oscillator to stabilise.

- **HIRCC Register − 11H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | HIRCO | HIRCF | HIRCEN |
| R/W | — | — | — | — | — | R/W | R | R/W |
| POR | — | — | — | — | — | 0 | 0 | 1 |

Bit 7~3 Unimplemented, read as "0"
Bit 2 **HIRCO**: HIRC clock output
This bit must be reserved at "0"

Bit 1 **HIRCF**: HIRC oscillator stable flag
0: Unstable
1: Stable
The HIRC stable time will spend 16 clocks when HIRCEN is enabled.

Bit 0 **HIRCEN**: HIRC oscillator enable control
0: Disable
1: Enable

• **HXTC Register − 12H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | — | — | HXTM | HXTF | HXTEN |
| R/W | — | — | — | — | — | R/W | R | R/W |
| POR | — | — | — | — | — | 0 | 0 | 0 |

Bit 7~3 Unimplemented, read as "0"

Bit 2 **HXTM**: HXT mode selection
0: HXT ≤ 10MHz – small sink/source current
1: HXT > 10MHz – large sink/source current
Note that if HXTEN=1, then changing this bit will have no effect.

Bit 1 **HXTF**: HXT oscillator stable flag
0: Unstable
1: Stable
When bit HXTEN is enable,this bit will be cleared to "0" and will be set after the HXT clock is stable.
The HXT stable time will spend some clock when bit HXTEN is enabled.

Bit 0 **HXTEN**: HXT oscillator enable control
0: Disable
1: Enable

## Input Signal Gain Control Amplifier – PGA

An internal programmable gain amplifier is provided to amplify the differential input signal before being converted. All input signals to the analog to digital converter must pass through the PGA. This pre-processing of the input signal enables an optimal signal range to be setup to obtain a converted value with optimal resolution.

### PGA Registers

The PGA is controlled using a series of registers to setup the gain value and also to select the input source.

• **PGAC0 Register − 01H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | VGS1 | VGS0 | AGS1 | AGS0 | PGS2 | PGS1 | PGS0 |
| R/W | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 Unimplemented, read as "0"

Bit 6~5 **VGS1~VGS0**: REFP/REFN differential reference voltage gain selection
00: VREFGN=1
01: VREFGN=1/2
10: VREFGN=1/4
11: Reserved

Bit 4~3 **AGS1~AGS0**: ADC converter PGAOP/PGAON differential input signal gain selection
00: ADGN=1
01: ADGN=2 (for Gain=128=PGAGN×ADGN=64×2)
10: Reserved
11: Reserved

Bit 2~0 **PGS2~PGS0**: PGA DI+/DI- differential channel input gain selection
000: PGAGN=1
001: PGAGN=2
010: PGAGN=4
011: PGAGN=8
100: PGAGN=16
101: PGAGN=32
110: PGAGN=64
111: Reserved

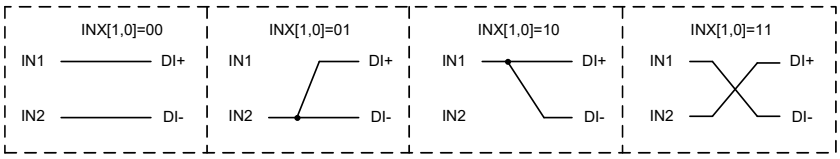
**• PGAC1 Register − 02H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | INIS | INX1 | INX0 | DCSET2 | DCSET1 | DCSET0 | — |
| R/W | — | R/W | R/W | R/W | R/W | R/W | R/W | — |
| POR | — | 0 | 0 | 0 | 0 | 0 | 0 | — |

Bit 7 Unimplemented, read as "0".

Bit 6 **INIS**: Selected input terminals IN1/IN2 internal connection
0: Not connected
1: Connected

Bit 5~4 **INX1, INX0**: The selected input ends ,IN1/IN2 and the PGA differential input ends, DI+/DI- connection control bits




Bit 3~1 **DCSET2~DCSET0**: Differential input signal PGAOP/PGAON offset selection
000: DCSET= +0V
001: DCSET= +0.25 × ΔVR_I
010: DCSET= +0.5 × ΔVR_I
011: DCSET= +0.75 × ΔVR_I
100: DCSET= +0V
101: DCSET= -0.25 × ΔVR_I
110: DCSET= -0.5 × ΔVR_I
111: DCSET= -0.75 × ΔVR_I
The voltage, ΔVR_I, is the differential reference voltage which is amplified by the specific gain selection based on the selected inputs.

Bit 0 Unimplemented, read as "0"

### PGA Input Channel Selection

In addition to the external analog input to be measured by the converter, there are several other internal analog voltage lines which can be connected to the converter. These come from a range of sources such as the temperature sensor and are normally used for calibration purposes.

**• PGACS Register − 03H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | CHSN2 | CHSN1 | CHSN0 | CHSP2 | CHSP1 | CHSP0 |
| R/W | — | — | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | — | — | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7~6 Unimplemented, read as "0"

Bit 5~3 **CHSN2~CHSN0**: PGA negative input end IN2 selection
000: AN1
001: AN3
010: Reserved
011: Reserved
100: $V_{DACO}$
101: $AV_{SS}$
110: $V_{CM}$
111: $V_{TSN}$ – Temperature sensor negative output

These bits are used to select the negative input, IN2. If the IN2 input is selected as a single end input, the $V_{CM}$ voltage must be selected as the positive input on IN1 for single end input applications. It is recommended that when the $V_{TSN}$ signal is selected as the negative input, the $V_{TSP}$ signal should be selected as the positive input for proper operations.

Bit 2~0 **CHSP2~CHSP0**: Positive input end IN1selection
000: AN0
001: AN2
010: Reserved
011: Reserved
100: $V_{DACO}$
101: Reserved
110: $V_{CM}$
111: $V_{TSP}$ – Temperature sensor positive output

These bits are used to select the positive input, IN1. If the IN1 input is selected as a single end input, the $V_{CM}$ voltage must be selected as the negative input on IN2 for single end input applications. It is recommended that when the $V_{TSP}$ signal is selected as the positive input, the $V_{TSN}$ signal should be selected as the negative input for proper operations.

## Analog to Digital Converter Operation

The analog to digital converter receives a differential analog signal from the PGA output and converts it using a Delta Sigma converter into a 24-bit digital value. The overall operation of the converter is controlled by a series of control registers.

### • ADCR0 Register − 07H

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | ADRST | ADSLP | ADOFF | ADOR3 | ADOR2 | ADOR1 | ADOR0 | VREFS |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **ADRST**: A/D converter software reset enable control
0: Disable
1: Enable

This bit is used to reset the A/D converter internal digital SINC filter. This bit is set low for A/D normal operations. However, if set high, the internal digital SINC filter will be reset and the current A/D converted data will be aborted. A new A/D data conversion process will not be initiated until this bit is set low again.

Bit 6 **ADSLP**: A/D converter sleep mode enable control
0: Normal mode
1: Sleep mode

This bit is used to determine whether the A/D converter enters the sleep mode or not when the A/D converter is powered on by setting the ADOFF bit low. When the A/D converter is powered on and the ADSLP bit is low, the A/D converter will operate normally. However, the A/D converter will enter the sleep mode if the ADSLP bit is set high as the A/D converter has been powered on. The whole A/D converter circuit will be switched off except the PGA and internal Bandgap circuit to reduce the power consumption and VCM start-up stable time.

Bit 5 **ADOFF**: A/D converter module power on/off control
0: Power on
1: Power off
This bit controls the power of the A/D converter module. This bit should be cleared to zero to enable the A/D converter. If the bit is set high then the A/D converter will be switched off reducing the device power consumption. As the A/D converter will consume a limited amount of power, even when not executing a conversion, this may be an important consideration in power sensitive battery powered applications.
It is recommended to set the ADOFF bit high before the device enters the IDLE/SLEEP mode for saving power. Setting the ADOFF bit high will power down the A/D converter module regardless of the ADSLP and ADRST bit settings.

Bit 4~1 **ADOR3~ADOR0**: A/D conversion oversampling rate selection
0000: Oversampling rate OSR=32768
0001: Oversampling rate OSR=16384
0010: Oversampling rate OSR=8192
0011: Oversampling rate OSR=4096
0100: Oversampling rate OSR=2048
0101: Oversampling rate OSR=1024
0110: Oversampling rate OSR=512
0111: Oversampling rate OSR=256
1000: Oversampling rate OSR=128
Others: Reserved

Bit 0 **VREFS**: A/D converter reference voltage pair selection
0: Internal reference voltage pair – $V_{CM}$ & $AV_{SS}$
1: External reference voltage pair – $V_{REFP}$ & $V_{REFN}$

**• ADCR1 Register − 08H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | FLMS2 | FLMS1 | FLMS0 | VRBUFN | VRBUFP | ADCDL | EOC | — |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | — |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — |

Bit 7~5 **FLMS2~FLMS0**: A/D converter clock divided ratio selection
000: $f_{ADCK}=f_{MCLK}/30$, N=30
010: $f_{ADCK}=f_{MCLK}/12$, N=12
Others: Reserved

Bit 4 **VRBUFN**: A/D converter negative reference voltage input (VRN) buffer control
0: Disable input buffer and enable bypass function
1: Enable input buffer and disable bypass function

Bit 3 **VRBUFP**: A/D converter positive reference voltage input (VRP) buffer control
0: Disable input buffer and enable bypass function
1: Enable input buffer and disable bypass function

Bit 2 **ADCDL**: A/D converted data latch function enable control
0: A/D converted data updated
1: A/D converted data not updated
If the A/D converted data latch function is enabled, the latest converted data value will be latched and not be updated by any subsequent converted results until this function is disabled. Although the converted data is latched into the data registers, the A/D converter circuits remain operational and EOC flag will not change state. It is recommended that this bit should be set high before reading the converted data in the ADRL, ADRM and ADRH registers. After the converted data has been read out, the bit must be cleared to zero to disable the A/D converter data latch function and allow further conversion values to be stored. In this way, the possibility of obtaining undesired data during A/D converter conversions can be prevented.
Note: Before reading the A/D converted data, the master application program needs to confirm that the ADCDL is 0 to indicate the existence of available data. Otherwise, the ADCDL bit should be cleared to 0 by the application program before continuing to poll the next available data.

Bit 1 **EOC**: End of A/D conversion flag
0: A/D conversion in progress
1: A/D conversion ended
This flag will be automatically set high by the hardware when a conversion process has completed but must be cleared by the application software.

Bit 0 Unimplemented, read as "0"

### A/D Data Rate Definition

The Delta Sigma ADC data rate can be calculated by the equation list below.

Data Rate = $f_{ADCK}$ / OSR

= ($f_{MCLK}$/N) / OSR

= $f_{MCLK}$ / (N×OSR)

$f_{ADCK}$: $f_{MCLK}$/N

$f_{MCLK}$: $f_{SYS}$ or $f_{SYS}$/2/(ADCK+1) using the ADCK bit field.

N: 30 or 12 determined by the FLMS bit field.

OSR: Oversampling rate determined by the ADOR field.

For example; if a data rate of 10Hz is desired. An $f_{MCLK}$ clock source with a frequency of 4.9152MHz ADC can be selected. Then set the FLMS field to “000” to obtain an “N” equal to 30. Finally, set the ADOR field to “0001” to select an oversampling rate equal to 16384. Therefore, the Data Rate = 4.9152MHz/(30×16384)=10Hz.

Note that the A/D converter has a notch rejection function for an AC power supply with a frequency of 50Hz or 60Hz when the data rate is equal to 10Hz.

### A/D Converter Clock Source

The clock source $f_{MCLK}$ for the A/D converter should be typically set to a value of 4.9152MHz, which originates from the system clock $f_{SYS}$. This can be chosen to be either $f_{SYS}$ or a subdivision of $f_{SYS}$. The division ratio value is determined by the ADCK4~ADCK0 bits in the ADCS register.

Internal OSC=4.9152MHz, $f_{ADCK}$=$f_{MCLK}$/30.

| Data Rate (Hz) | ADCK4~0 | ADOR3~0 | FLMS2~0 |
|---|---|---|---|
| 10 | 11111 | 0001 | 000 |

Internal OSC=4.9152MHz, $f_{ADCK}$=$f_{MCLK}$/12.

| Data Rate (Hz) | ADCK4~0 | ADOR3~0 | FLMS2~0 |
|---|---|---|---|
| 25 | 11111 | 0001 | 010 |

- **ADCS Register − 09H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | — | — | — | ADCK4 | ADCK3 | ADCK2 | ADCK1 | ADCK0 |
| R/W | — | — | — | R/W | R/W | R/W | R/W | R/W |
| POR | — | — | — | 0 | 0 | 0 | 0 | 0 |

Bit 7~5 Unimplemented, read as "0"

Bit 4~0 **ADCK4~ADCK0**: A/D converter clock source $f_{MCLK}$ divided ratio selection
00000~11110: $f_{MCLK}$=$f_{SYS}$/2/(ADCK[4:0] + 1)
11111: $f_{MCLK}$=$f_{SYS}$

• **ADCTE Register − 0AH**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

Bit 7~0 Reserved bits, should be fixed as 1110_0111B.

## A/D Operating Modes

The A/D Converter has four operating modes, which are the Normal mode, Power down mode, Sleep mode and Reset mode. These modes are controlled by a combination of the ADOFF, ADSLP and ADRST bits in the ADCR0 register as shown in the accompanying table. The ADOFF controls the overall on/off condition and if high will power down the A/D converter to reduce power. When the ADOFF bit is low, the converter will be powered on and the ADSLP bit will determine if the converter is in the normal operating mode or in the sleep mode.

| ADOFF | ADSLP | ADRST | Operating Mode | Description |
|---|---|---|---|---|
| 1 | x | x | Power down mode | Bandgap off, PGA off, ADC off, Temperature sensor off, VRN/VRP buffer off, SINC filter off |
| 0 | 1 | x | Sleep mode | Bandgap on, PGA on, ADC off, Temperature sensor off, VRN/VRP buffer off, SINC filter on |
| 0 | 0 | 0 | Normal mode | Bandgap on, PGA on, ADC on, Temperature sensor on/off, VRN/VRP buffer on/off, SINC filter on |
| 0 | 0 | 1 | Reset mode | Bandgap on, PGA on, ADC on, Temperature sensor on/off, VRN/VRP buffer on/off, SINC filter Reset |

"x" unknown

**A/D Operating Mode Summary**

Note: 1. The VCM generator (Bandgap) can be switched on or off by configuring the VCMEN bit.
2. The Temperature sensor can be switched on or off by configuring the CHSN[2:0] or CHSP[2:0] bits
3. The VRN buffer can be switched on or off by configuring the VRBUFN bit while the VRP buffer can be switched on or off by configuring the VRBUFP bit

## A/D Conversion Process

To enable the A/D Converter, the first step is to disable the ADC power down and sleep mode by clearing the ADOFF and ADSLP bits to make sure the A/D Converter is powered up. The ADRST bit in the ADCR0 register is used to start and reset the A/D converter after power on. To set ADRST bit from low to high and then low again, the A/D Converter is ready for operation. These three bits are used to control the overall start operation of the internal analog to digital converter.

The EOC bit in the ADCR1 register is used to indicate when the analog to digital conversion process is complete. This bit will be automatically set to "1" by the hardware after a conversion cycle has ended. The ADC converted data will be updated continuously by new converted data. If the ADC converted data latch function is enabled, the latest converted data will be latched and the following new converted data will be discarded until this data latch function is disabled.

The differential reference voltage supply to the A/D Converter can be supplied from either the internal power supply, VCM and AVSS, or from an external reference source supplied on pins VREFP and VREFN. The desired selection is made using the VREFS bit in the ADCR0 register.

### Summary of A/D conversion steps

- Step 1

  Enable the power VCM for PGA and ADC.

- Step 2

  Select the PGA, ADC, reference voltage gains by PGAC0 register

- Step 3

  Select the PGA settings for input connection and DCSET option by PGAC1 register

- Step 4

  Select the required A/D conversion clock source 4.9152MHz by correctly programming bits ADCK4~ADCK0 in the ADCS register.

- Step 5

  Select output data rate by cofiguring the ADOR[2:0] bits in the ADCR0 register and FLMS[2:0] bits in the ADCR1 register.

- Step 6

  Select which channel is to be connected to the internal PGA by correctly programming the CHSP2~CHSP0 and CHSN2~CHSN0 bits which are also contained in the PGACS register.

- Step 7

  Release the power down mode and sleep mode by clearing the ADOFF and ADSLP bits in ADCR0 register.

- Step 8

  Reset the A/D by setting the ADRST to high in the ADCR0 register and clearing this bit to zero to release reset status.

- Step 9

  To check when the analog to digital conversion process is complete, the EOC bit in the ADCR1 register can be polled. The conversion process is complete when this bit goes high. When this occurs the A/D data registers ADRL, ADRM and ADRH can then be read to obtain the conversion value.

### A/D Transfer Function

As the converted value is 24-bits its full-scale converted digitised value has a decimal value of 8388607 to -8388608. The converted data format is formed by a two's complement binary value. The MSB of the converted data is the signed bit. Since the full-scale analog input value is equal to the amplified value of the VCM or differential reference input voltage, ΔVR_I, selected by the VREFS bit in ADCR0 register, this gives a single bit analog input value of ΔVR_I divided by 8388608.

$$1\ LSB = \Delta VR\_I / 8388608$$

The A/D Converter input voltage value can be calculated using the following equation:

$$\Delta SI\_I = (PGAGN \times ADGN \times \Delta DI\pm) + DCSET$$

$$\Delta VR\_I = VREFGN \times \Delta VR \pm$$

$$ADC\_Conversion\_Data = (\Delta SI\_I / \Delta VR\_I) \times K$$

Where K is equal to $2^{23}$.

Note: 1. The PGAGN, ADGN, VREFGN values are determined by the PGS, AGS, VGS control bits.
2. ΔSI_I is the differential input signal after amplification and offset adjustment
3. PGAGN: Programmable Gain Amplifier gain

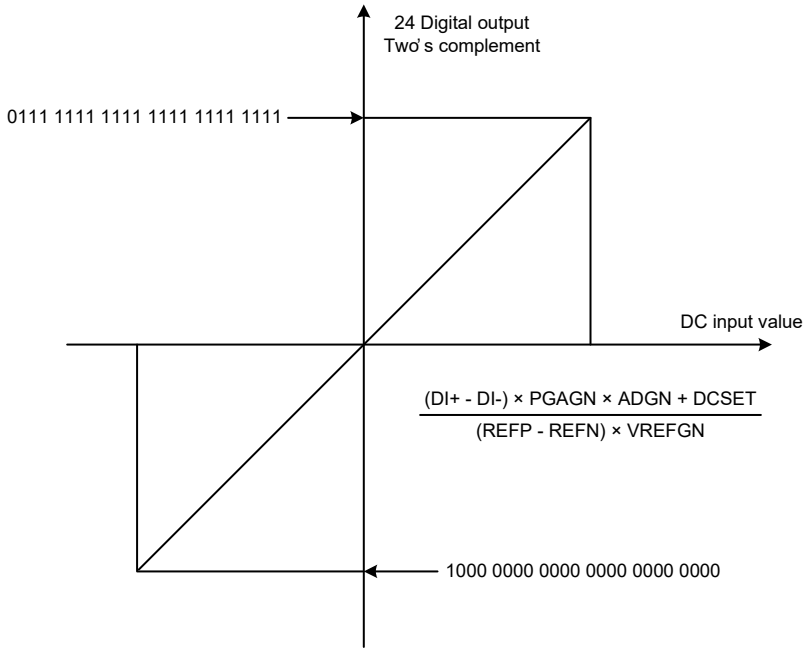
4. ADGN: A/D Converter gain
5. VREFGN: Reference voltage gain
6. ΔDI±: Differential input signal derived from external channels or internal signals
7. DCSET: Offset voltage
8. ΔVR±: Differential reference voltage
9. ΔVR_I: Differential reference input voltage after amplification

Due to the digital system design of the converter, the maximum A/D converted value is 8388607 and the minimum value is -8388608, therefore the centre value is 0. The ADC_Conversion_Data equation illustrates this range of converted data variation.

| Converted Data 2's compliment Hex value | Decimal Value |
|---|---|
| 0x7FFFFF | 8388607 |
| 0x800000 | -8388608 |

**A/D Conversion Data Range**

The following diagram shows the relationship between the DC input value and the ADC converted data which is presented in Two's Complement format.




## A/D Converted Data

The A/D converter data is stored in three individual registers, ADRL, ADRM and ADRH. The converted data is related to the input voltage and the PGA selection setup and is generated in a two's complement binary code format. The length of this output code is 24 bits and the MSB is a signed bit. When the MSB is "0", this indicates that the input is "positive", while if the MSB is "1", this indicates that the input is "negative". The maximum value is 8388607 and the minimum value is -8388608. If the input signal exceeds the maximum value, the converted data is limited to 8388607, and if the input signal is less than the minimum value, the converted data is limited to -8388608.

• **ADRL Register − 04H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R | R | R | R | R | R | R | R |
| POR | x | x | x | x | x | x | x | x |

Bit 7~0 A/D conversion data register bit 7~bit 0

• **ADRM Register − 05H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R/W | R | R | R | R | R | R | R | R |
| POR | x | x | x | x | x | x | x | x |

Bit 7~0 A/D conversion data register bit 15~bit 8

• **ADRH Register − 06H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| R/W | R | R | R | R | R | R | R | R |
| POR | x | x | x | x | x | x | x | x |

Bit 7~0 A/D conversion data register bit 23~bit 16

### Converting the Digital Value to a Voltage

The analog voltage value can be recovered using the following equations:

If the MSB=0 for positive value converted data:

$$\text{Input Voltage} = \frac{(\text{Converted\_data}) \times \text{LSB} - \text{DCSET}}{\text{PGA} \times \text{ADGN}}$$

If the MSB=1 for negative converted data:

$$\text{Input voltage} = \frac{(\text{Two's\_complement\_of\_Converted\_data}) \times \text{LSB} - \text{DCSET}}{\text{PGA} \times \text{ADGN}}$$

Note: Two's complement=One's complement +1

### Temperature Sensor

The device includes a fully internal temperature sensor to allow for compensation due to temperature effects. By selecting the PGA input channels to VTSP and VTSN signals, the A/D Converter can obtain temperature information and then use the result to compensate the A/D converted data to minimise the effects of temperature.

### Effective Number of Bits – ENOB

Although the analog to digital converter is a 24-bit type various factors such as the PGA gain and the data rate affect the actual number of effective number of converted bits.

## Programming Considerations

During microcontroller operations where the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption, by setting bit ADOFF high in the ADCR0 register. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines.

When writing to the DAC registers, DAH and DAL, note that this must be carried out in a special sequence. This is because when writing to the DAL register, the data is only written into a shadow buffer register. Only when data is written to the DAH register will data in the shadow buffer be transferred to the DAL register. Therefore when writing data to the DAC registers first write data to the DAL register and then to the DAH register.

## External Interface Communication

The device communicates with external hardware using its internal I²C interface. Originally developed by Philips, the I²C interface is a two line low speed serial interface for synchronous serial data transfer. With the advantage of only two lines for communication, a relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.

### I²C Interface Operation

The I²C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus. When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus, and it is only the master that will drive the SCL clock line. This device only operates in the slave mode, and will therefore only operate in response to the master. There are two methods for this device to transfer data on the I²C bus, the slave transmit mode and the slave receive mode.

Several registers control the overall operation of the I²C bus interface.

### I²C Address and Register Write/Read

#### I²C Address Selection

As this device only operates as a slave, and as it may be connected to a common I²C bus along with other I²C devices, it will require a specific address for it to be communicated to by the external master. The address of the device is setup using the A1 and A2 pins which allows for 4 different address values.

If pin XTSB is 0, pin OSC1/A1 is functioned as OSC1, OSC2/A2 is functioned as OSC2, and I²C address is 0xA0.

If pin XTSB is 1, pin OSC1/A1 is functioned as A1, OSC2/A2 is functioned as A2, and I²C address depends on [A2:A1],

00 → 0xA0, 01 → 0xB0

10 → 0xC0, 11 → 0xD0

Note: 8-pin package I²C address is fixed at 0xD0.

| XTSB Pin | OSC2/A2 | OSC1/A1 | I²C Address |
|---|---|---|---|
| 0 | OSC2 | OSC1 | 0xA0 |
| 1 | A2 | A1 | 00 → 0xA0<br>01 → 0xB0<br>10 → 0xC0<br>11 → 0xD0 |

• **SIMC0 Register − 0EH**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SIMS | — | — | — | SIMDEB1 | SIMDEB0 | — | — |
| R/W | R/W | — | — | — | R/W | R/W | — | — |
| POR | 0 | — | — | — | 0 | 0 | — | — |

Bit 7 **SIMS**
0: Normal operation
1: Results in unpredictable behavior
This bit must be kept at a zero value for normal operation

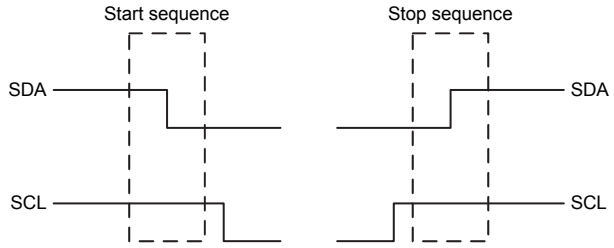
Bit 6~4 Unimplemented, read as "0"

Bit 3~2 **SIMDEB1~SIMDEB0**: I²C debounce time selection
00: No debounce
01: 2 system clock debounce
10: 4 system clock debounce
11: 4 system clock debounce

Bit 1~0 Unimplemented, read as "0"

### Start and Stop Operations

Normally the SDA line can only change when the SCL line is low. There are two exceptions however and that is for the Start and Stop operations, where the SCL line will be forced high by the master and the SDA line will change sate. As the diagram shows when the SCL line is high, a high to low SDA line transition indicates a start operation and a low to high SDA line transition indicates a stop operation.




### I²C Bus Data Transfer

Data is transferred on the I²C bus in 8 bit packets, first transmitting the MSB which is the most significant bit and lastly the LSB bit, the least significant bit. When the data has been setup on the SDA line, the SCL line then generates a high pulse to latch the data. When the SCL line is high the SDA line is not permitted to change state. After 8-bits have been transmitted, the device will then send a 9th bit which is the acknowledge bit. Therefore in total there are 9 bits transmitted and subsequently 9 SCL clock pulses to transfer each 8-bits or byte of data. When the receiving device sends back a low ACK bit, this is to acknowledge that it has received the 8-bits of data and is ready to receive another byte. If a high ACK bit is sent back, this indicates that it is unable to receive any further data and the master should then send a stop sequence.

### I²C Register Write/Read

• **Write Process**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start | Device Address | | | | | | | | Write | ACK | Register Address | | | | | | | | ACK | Register Data | | | | | | | | ACK | Stop |

• **Read Process**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start | Device Address | | | | | | | Write | ACK | Register Address | | | | | | | | ACK | Start | Device Address | | | | | | | Read | ACK | Register Data | | | | | | | | ACK | Stop |

### I²C Bus Start Signal

The START signal can only be generated by the master device connected to the I²C bus and not by the slave device. This START signal will be detected by all devices connected to the I²C bus. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

### Slave Address

The transmission of a START signal by the master will be detected by all devices on the I²C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal.

### I²C Bus Slave Address Acknowledge Signal

After the master has transmitted a calling address, any slave device on the I²C bus, whose own internal address matches the calling address, must generate an acknowledge signal. The acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication.

### I²C Bus Data and Acknowledge Signal

The transmitted data is 8-bits wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8-bits of data, the receiver must transmit an acknowledge signal, level 0, before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus.

### I²C Timeout Function

The I²C interface includes a timeout function which is controlled by a single register. This register sets the overall enable/disable function as well as the timeout value in system clock units. Determining whether the I²C bus has timed out is implemented by reading the SIMTOF bit. This bit will be automatically set high when the I²C bus times out, but needs to be cleared manually by the application program.

• **SIMTOC Register − 10H**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | SIMTOEN | SIMTOF | SIMTOS5 | SIMTOS4 | SIMTOS3 | SIMTOS2 | SIMTOS1 | SIMTOS0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| POR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 **SIMTOEN**: I²C time-out control
0: Disable
1: Enable

Bit 6 **SIMTOF**: I²C time-out flag
0: Not occurred
1: Occurred
The bit is set by time-out function and is cleared by the application program.

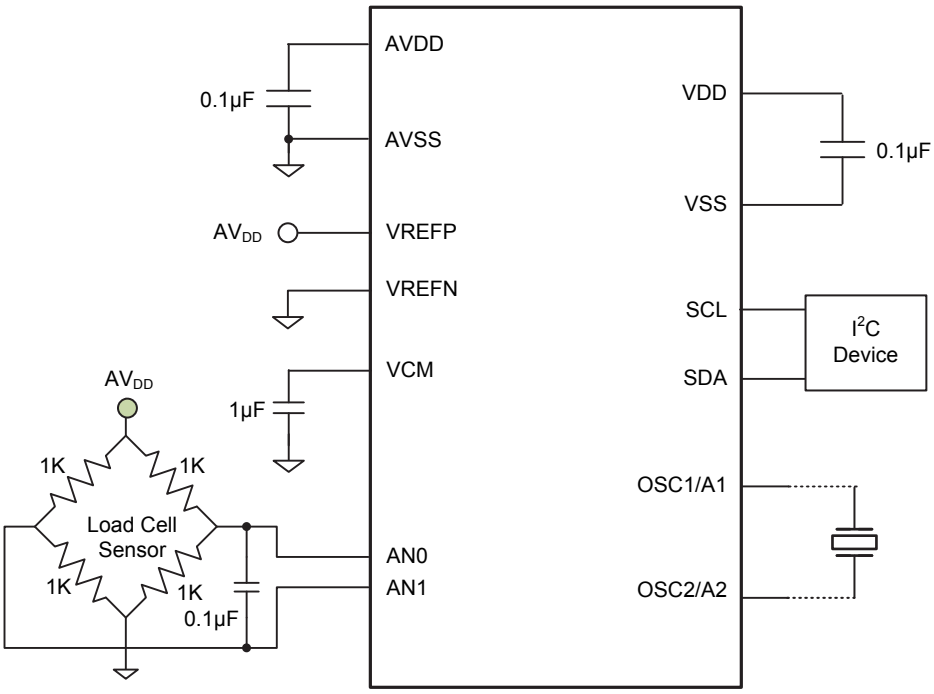
Bit 5~0 **SIMTOS5~SIMTOS0**: $I^2C$ time-out selection time

The $I^2C$ Time-Out clock source is $f_{SUB}/32$. ($f_{SUB}=f_{SYS}/128$)

The $I^2C$ Time-Out time is ([SIMTOS5:SIMTOS0]+1) × ($32/f_{SUB}$)

Note: The time-out mechanism should be enabled by setting the SIMTOEN bit to 1, as its default value is 0, to avoid abnormal functions of the $I^2C$ due to interference. When a time-out occurs, the SIMTOF flag will be set to 1, and the SIMTOEN bit will be automatically cleared to 0 by the hardware. Therefore, the SIMTOEN bit must be set to 1 again by the application program.

## Application Circuits



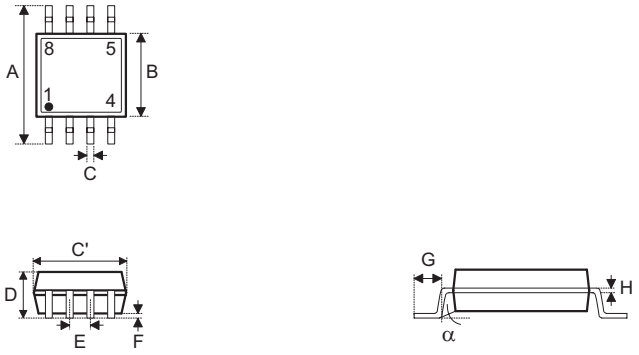
## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

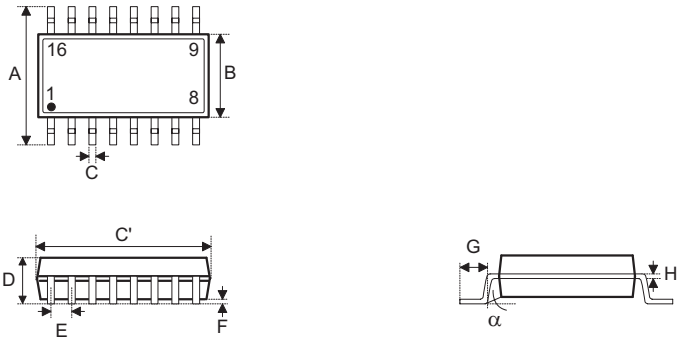
## 8-pin SOP (150mil) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | | 0.236 BSC | |
| B | | 0.154 BSC | |
| C | 0.012 | — | 0.020 |
| C′ | | 0.193 BSC | |
| D | — | — | 0.069 |
| E | | 0.050 BSC | |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | | 6.00 BSC | |
| B | | 3.90 BSC | |
| C | 0.31 | — | 0.51 |
| C′ | | 4.90 BSC | |
| D | — | — | 1.75 |
| E | | 1.27 BSC | |
| F | 0.10 | — | 0.25 |
| G | 0.40 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |

### 16-pin NSOP (150mil) Outline Dimensions




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | | 0.236 BSC | |
| B | | 0.154 BSC | |
| C | 0.012 | — | 0.020 |
| C' | | 0.390 BSC | |
| D | — | — | 0.069 |
| E | | 0.050 BSC | |
| F | 0.004 | — | 0.010 |
| G | 0.016 | — | 0.050 |
| H | 0.004 | — | 0.010 |
| α | 0° | — | 8° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | | 6.00 BSC | |
| B | | 3.90 BSC | |
| C | 0.31 | — | 0.51 |
| C' | | 9.90 BSC | |
| D | — | — | 1.75 |
| E | | 1.27 BSC | |
| F | 0.10 | — | 0.25 |
| G | 0.40 | — | 1.27 |
| H | 0.10 | — | 0.25 |
| α | 0° | — | 8° |